Remarks

Claims 1-23 are pending in the present application. Unelected claims 1-6 and 16-23 have been canceled herein without prejudice pending the filing of a divisional application. Claims 7-15 remain in the present application and are now pending in the present application. Claims 24-34 are added herein to further recite additional embodiments of the invention. Reconsideration is requested.

Applicant affirms the provisional election made telephonically by attorney Brian Carlson on November 19, 2004, to Group II, claims 7-15. Therefore the claims grouped under Group I are canceled herein pending the filing of a divisional application.

Examiner rejected claims 7-9 and 12-15 under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 6,335,249, to Thei, et al. ("Thei '249"). Applicant respectfully traverses this rejection.

The Examiner asserts that each method step of Claim 7 is described in the Thei '249 reference. In particular, the Examiner identified certain lines of Column 5 for providing the well of Claim 7, the step of removing a portion of the STI element to form STI regions opposing an exposed portion of the well, and the Examiner identified certain lines of Column 7 as providing the step of forming a floating node in the exposed portion of the well.

Applicant respectfully responds that the relied upon reference does not provide the claimed method steps.

Claim 7 recites:

> A method of manufacturing a photodiode sensor, comprising:
>
> forming a well in a substrate;

forming a shallow trench isolation (STI) element at least partially in the well;

removing a portion of the STI element to form STI regions opposing an exposed portion of the well;

forming a floating node in the exposed portion of the well;

forming a borderless contact buffer layer over at least the floating node and along sidewalls of the STI regions;

forming an interlevel dielectric layer over the borderless contact buffer layer; and

forming a borderless contact extending through the interlevel dielectric layer and the borderless contact layer to the floating node.

The Thei '249 provides an improved method for forming a borderless contact structure to silicide FET transistors. The borderless contact is formed through an interlevel dielectric layer to a silicide layer overlying a source/drain region. The borderless contact is formed adjacent one side of an STI region.

Thei '249 does not show or teach the method of forming a photodiode as recited in Claim 7, in particular there is at least no teaching found of at least the steps of:

forming a well in a substrate;

removing a portion of the STI element to form STI regions opposing an exposed portion of the well;

and

forming a floating node in the exposed portion of the well;

The Examiner referred to text in Column 5 of the Thei '249 reference for support for the assertion that the reference anticipates the step of forming a well. However, the text referred to has been examined closely and no teaching is found for a well in the substrate. The figures do not depict a well, and no reference to a well is found anywhere in the Thei '249 reference.

With respect to the step of removing a portion of the STI element to form STI regions opposing an exposed portion of the well, the reference does not provide this element, either. The STI in Thei '249 is exposed at one end; however, it is not removed to form STI regions (plural regions, requiring that the removal step be more than a step exposing one end of an existing single structure) opposing an exposed portion of the well (again, requiring the resulting STI regions be plural regions opposing another region, not a single structure). In fact a comparison of Thei '249 Figures 2 and 3 reveal that the STI is not removed at all, instead, the reference removes layer 19 adjacent the end of the STI 12, and exposes one end of a structure, no STI is removed.

With respect to forming a floating node in the exposed portion of the well, the reference also fails to teach this step. The structure the Examiner asserts is formed by the Thei '249 patent is the deep implant G, which is part of an electrically active element, the source/drain n-p junction 19 structures (Thei '249, Col. 7, lines 45-50). The source drain structure is electrically coupled to other structures, specifically it is electrically coupled to the drain/source structure when the gate electrode is at potential over the threshold, operates the current conduction path of the N-FET transistor shown in Figures 2-4 of Thei '249. Thus region G of Thei '249 is not a floating node, as required, as it does not float. It is the source drain region of an N-FET transistor.

Thus, Applicant submits that the reference cited by the Examiner does not anticipate the method steps of Claim 7, that Claim 7 is therefore novel and unobvious over the reference and allowable. Reconsideration and allowance are respectfully requested.

Claims 8-10 depend from and recite additional steps not shown in the reference, and further add steps to the method of Claim 7. As Claim 7 is believed to be allowable, these dependent claims are also believed to be allowable. Reconsideration and allowance are therefore requested.

Claims 12-15 were also rejected over the Thei '249 Patent. These claims also depend from and incorporate the steps of Claim 7, and add additional patentable steps to the method of Claim 7. As Claim 7 is believed to be allowable, these additional method claims are also believed to be allowable. Reconsideration and allowance are therefore requested.

Claims 10 and 11 were objected to as depending from a rejected claim, but indicated as reciting allowable limitations. Applicant acknowledges the finding of allowability of these claims. As these claims depend from Claim 7, which is believed to be allowable, these dependent claims are also believed to be allowable. Accordingly, reconsideration and allowance are requested.

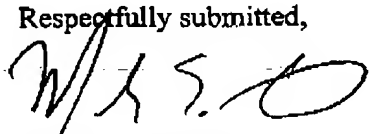
Newly submitted claims 24-34 also recite method steps of the invention that are allowable over the prior art. For example, Claim 25 recites a method for forming a photodiode with steps recited for forming layers having certain refractive indexes such that the impinging light will pass through materials having increasing indexes of refraction. Claims 25-31 depend from and recite additional steps on the method of Claim

25. Similarly, Claim 32 recites a method for forming a photodiode with layers formed having indexes of refraction in specific ranges. Claims 33-34 depend from and recite additional steps on the method of Claim 32. These new claims are believed to be allowable over the prior art. Consideration and allowance are therefore requested.

The amendment and remarks herein are believed to be fully responsive to the Examiner's Office Action and to place the application in a condition for allowance.

Applicant respectfully request that the present application be passed to issuance. Please contact Applicant's attorney with any questions regarding this matter.

Respectfully submitted,



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